Access DB# 677563
1/8

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: P. Laufer Examiner# : _____ Date: 5/28/02

Art Unit: 2100 Phone Number: 306-4160 Serial Number: 10/084757

Mail Box and Bldg/Room Location: _____ Results Format Preferred (circle): Paper Disk E-mail

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

_____

Earliest Priority Filing Date: _____

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

5,970,255

****

STAFF USE ONLY

Searcher: A Green

Searcher Phone: 6-4767

Searcher Location: 4B40

Date Searcher Picked Up: 5/28/02

Date Completed: 5/31/02

Searcher Prep & Review Time: 5

Clerical Prep Time: _____

Online Time: 15

Type of search

NA Sequence (#) _____

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Litigation ✓

Full Text _____

Patent Family _____

Other _____

Vendors and cost where applicable

STN _____

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1 of 1 DOCUMENT

5,970,255

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Oct. 19, 1999

System for coupling programmable logic device to external circuitry which selects a logic standard and uses buffers to modify output and input signals accordingly

REISSUE:
Reissue Application filed Oct. 19, 2001 (O.G. May 21, 2002) Ex. Gp.: 2782; Re. S.N. 10/084,757

INVENTOR:
Tran, Nghia, San Jose, California
Li, Ying Xuan, Santa Clara, California
Balicki, Janusz, San Jose, California
Costello, John, San Jose, California

ASSIGNEE-AT-ISSUE:
Altera Corporation, San Jose, California (02)

APPL-NO:
543,649

FILED:
Oct. 16, 1995

INT-CL:
[6] G06F 13#10

US-CL:
395#893; 395#828; 395#830; 395#834; 395#882; 395#884

SEARCH-FLD:
326#44, 71, 75, 81, 83, 108, 38, 41, 73, 86; 365#229, 185.14; 340#825.8; 380#3; 395#569, 828, 830, 834, 882, 884, 893; 327#333; 375#377; 711#103, 104

PRIM-EXMR:
Lee, Thomas C.

ASST-EXMR:
Yuan, Chien

LEGAL-REP:
Fish & Neave
Morris; Robert W.
Shanahan; Michael F.

No Documents Found

No documents were found for your search (**5970255 or 5,970,255**). Please edit your search and try again. You may want to try one or more of the following:

- Check for spelling errors.
- Remove some search terms.
- Use more common search terms.
- If applicable, look for all dates.

Edit Search

LEXIS-NEXIS
Library: PATENT
File: CASES

No Documents Found

No documents were found for your search (**5970255 or 5,970,255**). Please edit your search and try again. You may want to try one or more of the following:

- Check for spelling errors.
- Remove some search terms.
- Use more common search terms.
- If applicable, look for all dates.

Edit Search

LEXIS-NEXIS
Library: PATENT
File: JNLS

?us5970255/pn

** SS 3: Results 1

Search statement 4

?prt full nonstop legalall

1/1 PLUSPAT - (C) QUESTEL-ORBIT
PN - US5970255 A 19991019 [US5970255]
TI - (A) System for coupling programmable logic device to external circuitry which selects a logic standard and uses buffers to modify output and input signals accordingly
PA - (A) ALTERA CORP (US)
IN - (A) TRAN NGHIA (US); LI YING XUAN (US); BALICKI JANUSZ (US); COSTELLO JOHN (US)
AP - US54364995 19951016 [1995US-0543649]
PR - US54364995 19951016 [1995US-0543649]
IC - (A) G06F-013/10
EC - G11C-007/10M7
- G11C-007/10R
- H03K-019/177
PCL - ORIGINAL (O) : 710073000; CROSS-REFERENCE (X) : 710008000 710010000 710014000 710062000 710064000
DT - Basic
CT - USRe34444; US4032800; US4609986; US4617479; US4677318; US4713792; US4774421; US4871930; US4899067; US4912342; US4972470; US4975602; US4987578; US4994691; US5003200; US5023488; US5101122; US5121006; US5121359; US5220214; US5235219; US5260610; US5260611; US5350954; US5371422; US5374858; US5412599; US5426744; US5428305; US5483178; US5534798; US5590305; US5600267; US5732407
- R.C. Minnick, "A Survey of Microcellular Research," Journal of the Association for Computing Machinery, vol. 14, No. 2, pp. 203-241, Apr. 1967.

S.E. Wahlstrom, "Programmable Logic Arrays--Cheaper by the Millions," Electronics, Dec. 11, 1967, pp. 90-95.

Recent Developments in Switching Theory, A. Mukhopadhyay, ed., Academic Press, New York, 1971, chapters VI and IX, pp. 229-254 and 369-422.
STG - (A) United States patent
AB - A programmable input/output device for use with a programmable logic device (PLD) is presented comprising an input buffer, an output buffer and programmable elements. The programmable elements may be programmed to select a logic standard for the input/output device to operate at. For instance, a given set of Select Bits applied to the programmable elements may select TTL logic, in which case the input and output buffers would operate according to the voltage levels appropriate for TTL logic (e.g., 0.4 volts to 2.4 volts). For a different set of Select Bits, the GTL logic standard would be applied (e.g., 0.8 volts to 1.2 volts). The invention enables a single PLD to be used in conjunction with various types of external circuitry.

1/1 LGST - (C) LEGSTAT
PN - US 5970255 [US5970255]
AP - US 543649/95 19951016 [1995US-0543649]
DT - US-P
ACT - 19951016 US/AE-A
APPLICATION DATA (PATENT)

{US 543649/95 19951016 [1995US-0543649]}
- 19991019 US/A
PATENT
UP - 1999-46

1/1 CRXX - (C) CLAIMS/RRX
PN - 5,970,255 A 19991019 [US5970255]
PA - Altera Corp
ACT - 20011019 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20020521
REISSUE REQUEST NUMBER: 10/084757
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2782

Reissue Patent Number:

1/1 PAST - (C) Thomson Derwent
AN - 200221-002011
PN - 5970255 A [US5970255]
OG - 2002-05-21
ACT - REISSUE APPLICATION FILED

fam us5970255/pn

1 Patent Groups
** SS 2: Results 1

Search statement 3

?famstate nonstop

1/1 INPADOC - (C) INPADOC
PN - US 5970255 A 19991019 [US5970255]
TI - SYSTEM FOR COUPLING PROGRAMMABLE LOGIC DEVICE TO EXTERNAL CIRCUITRY WHICH SELECTS A LOGIC STANDARD AND USES BUFFERS TO MODIFY OUTPUT AND INPUT SIGNALS ACCORDINGLY
IN - TRAN NGHIA [US]; LI YING XUAN [US]; BALICKI JANUSZ [US]; COSTELLO JOHN [US]
PA - ALTERA CORP [US]
AP - US 543649/95-A 19951016 [1995US-0543649]
PR - US 543649/95-A 19951016 [1995US-0543649]
IC - G06F-013/10

1/1 LEGALI - (C) LEGSTAT
PN - US 5970255 [US5970255]
AP - US 543649/95 19951016 [1995US-0543649]
DT - US-P
ACTE- 19951016 US/AE-A
APPLICATION DATA (PATENT)
{US 543649/95 19951016 [1995US-0543649]}
- 19991019 US/A
PATENT
UP - 1999-46